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PTO/SB/08A (08-00)

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Substitute for Form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Complete If Known	
				Application Number	
				Filing Date	
				First Named Inventor	
				Group Art Unit	
				Examiner Name	
Sheet	1	of	2	Attorney Docket No.	TI-33887.1

U.S. PATENT DOCUMENTS						
Exam. Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
	AA	5,785,236		Cheung, et al.	07/28/1998	
	AB	6,213,347 B1		Thomas	04/10/2001	
	AC	6,228,680 B1		Thomas	05/08/2001	
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	AE	09/775,322		Stierman, et al.	02/01/2001	
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	AG					
	AH					
	AI					
	AJ					
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FOREIGN PATENT DOCUMENTS							
Exam. Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Office ³	Number ⁴	Kind Code ² (if known)			
	BA		JP 1-209746		Moriyama Yoshifumi	23/08/1989	
	BB						
	BC						
	BD						
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	BF						
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	BH						
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Substitute for Form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Complete If Known			
		Application Number			
		Filing Date			
		First Named Inventor	<i>Christo P. Bojkov, et al.</i>		
		Group Art Unit			
		Examiner Name	<i>Lucia, Monica</i>		
Sheet	2	of	2	Attorney Docket No.	<i>TI-33887.1</i>

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Exam. Initials ¹	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	CA	"A Silicon and Aluminum Dynamic Memory Technology", Richard A. Larsen, IBM J. Res. Develop., Vol. 24, No. 3, 05/1980, pp. 268-282	
	CB	"Controlled Collapse Reflow Chip Joining", L. F. Miller, IBM J. Res. Develop., Vol. 13, 05/1969, pp. 239-250	
	CC	"Geometric Optimization of Controlled Collapse Interconnections", L. S. Goldman, IBM J. Res. Develop., Vol. 13, 05/1969, pp. 251-265	
	CD	"Parametric Study of Temperature Profiles in Chips Joined by Controlled Collapse Techniques", Sevgin Oktay, IBM J. Res. Develop., Vol. 13, 05/1969, pp. 272-285	
	CE	"Reliability of Controlled Collapse Interconnections", K. C. Norris and A. H. Landzberg, IBM J. Res. Develop., Vol. 13, 05/1969, pp. 266-271	
	CF	"SLT Device Metallurgy and its Monolithic Extension", P. A. Totta and R. P. Sopher, IBM J. Res. Develop., Vol. 13, 05/1969, pp. 226-238	
	CG	"Studies of the SLT Chip Terminal Metallurgy", B. S. Berry and I. Ames, IBM J. Res. Develop., Vol. 13, 05/1969, pp. 286-296	
	CH		
	CI		
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	CK		
	CL		
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INFORMATION DISCLOSURE CITATION
U.S. PATENT DOCUMENTS

<u>Examiner Initial</u>	<u>Document Number</u>	<u>Date</u>	<u>Name</u>	<u>Class</u>	<u>Subclass</u>
	5,656,858	8/1997	Kondo et al.	257	737
	6,133,136	10/2000	Edelstein et al.	438	618
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<u>JP401094641A</u>	<u>4/1989</u>	<u>Kikkai</u>
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OTHER DOCUMENTS